A 5GHz 56dB Voltage Gain 0.18μm CMOS LNA with Built-in Tunable Channel Filter for Direct Conversion 802.11a Wireless LAN Receiver

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Abstract — **A 5GHz, 56dB voltage gain Low Noise Amplifier with built-in tunable center frequency and 30MHz bandwidth channel selection filter was implemented using 0.18μm CMOS process. Using compact high quality-factor 3-dimensional solenoid on-chip inductors, the LNA drains 0.9mA current from the 1.5V power supply and has 6.5dB noise figure. The power consumption can be further reduced if a smaller gain is desirable.**

I. Introduction

Direct conversion architecture offers the potential benefit of low cost and low power to the 5GHz wireless LAN system. Works[1] have been done to improve the performance. However, as most signal amplification and channel selection filtering of the receiver are carried out at the baseband frequency, it still suffers from low sensitivity and low dynamic range. One way to overcome this limitation is to increase the RF signal gain and put a channel selection filter before the mixer.

Fig. 1 shows the block diagram of a direct conversion receiver. Typical LNA gain is limited to 20dB to avoid the mixer being saturated by strong interferences. Interference suppression is mainly done by the lowpass filter at a later stage. However, this LNA gain is not large enough to suppress the DC-offset created by the local oscillator signal self-mixing and the flicker noise of both the baseband amplifier and the lowpass filter. If a high gain LNA is used, a high quality-factor, or narrow bandwidth, channel selection bandpass filter is required to allow only in-channel signal to pass through and reject the adjacent channel signals or out-band interference. However, the LC-tank at the LNA output using an on-chip inductor has limited Q-factor for narrow bandwidth channel selection filter requirement. An external high-Q bandpass filter, like the SAW filter, can be inserted between the LNA and the mixer. However, the increased power consumption and cost make it less attractive. In addition, it is only useful for band filtering or fixed channel application.

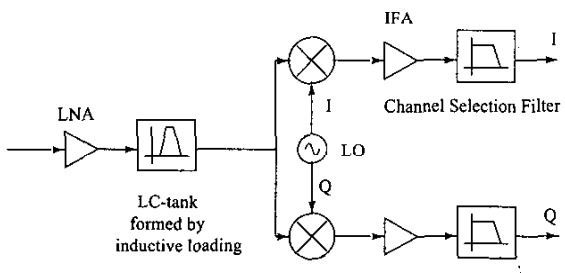

Fig. 1 Block diagram for simple direct conversion receiver.

II. Circuit Implementation

The Q-factor enhancement technique[2] for inductor is used to increase the effective Q-factor of the LC-tank and hence reduce the filter bandwidth to meet the channel bandwidth requirement. The amplifier gain at the resonant frequency is proportional to the Q-factor of the LC-tank. Increased effective Q-factor of the LC-tank also boosts up the LNA gain at the resonant frequency significantly with little extra power consumption.The schematic of the LNA is shown in Fig. 2. A cross-coupled NMOS pair was used to enhance the Q-factor of the LC-tank. For the 802.11a wireless LAN system, each channel occupies a 16.6MHz frequency space. The channel spacing is 20MHz. A 30MHz filter bandwidth is chosen in our design to give some margin for center frequency offset and to attain a smaller in-channel gain variation. For a 30MHz filter bandwidth at 5.25GHz, the effective Q-factor of the LC-tank required is 175. The Q-factor of a typical on-chip inductor is one order of magnitude smaller than this target value. The amount of the negative transconductance provided by the Q-enhancement stage is approximately equal to the real part admittance of the LC-tank, which is inversely proportional to the product of inductance and Q-factor. Therefore, it is important to have both high inductance and starting Q-factor in order to minimize the current consumed and the noise injected by the Q-enhancement stage.

A compact, high quality-factor vertical solenoid inductor was used in our design. The inductance is 4.8nH, the Q-

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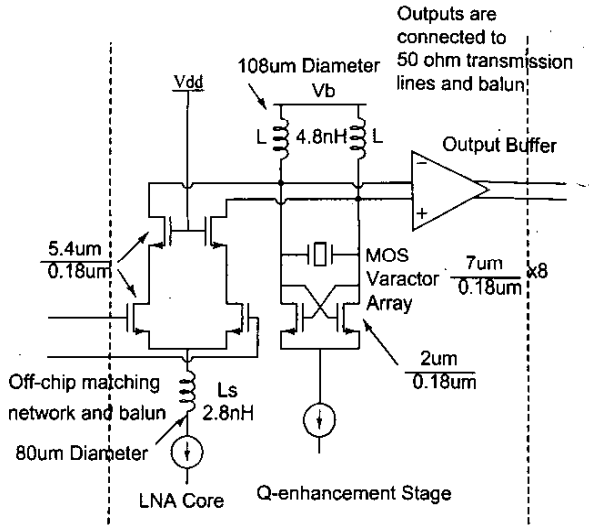

Fig. 2 The schematic of the LNA.

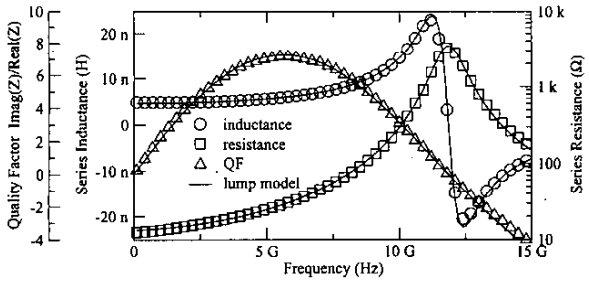

Fig. 3 The impedance and QF of the 4.8nH solenoid inductor. At the frequency higher than the self-resonant frequency of the inductor indicated by the negative QF, the inductor functions like a capacitor and is no longer useful. The simple RLC circuit with frequency dependent resistor can be closely matched to the measurement data.

factor at 5.25GHz is 7 and the self-resonant frequency is about 12GHz. The characteristic of the inductor is shown in Fig. 3. The 6-layer vertical solenoid inductor structure reduces the parasitic capacitance and allows us to achieve high inductance and self-resonant frequency simultaneously. The cross-section view of the inductor is shown in Fig. 4 together with the planar spiral inductor. The finite channel resistance of the input transistors provides the real part impedance for the input impedance matching. The inductor Ls shown in Fig. 2 is used to de-tune the common mode frequency response of the LNA to provide a better common mode noise rejection.

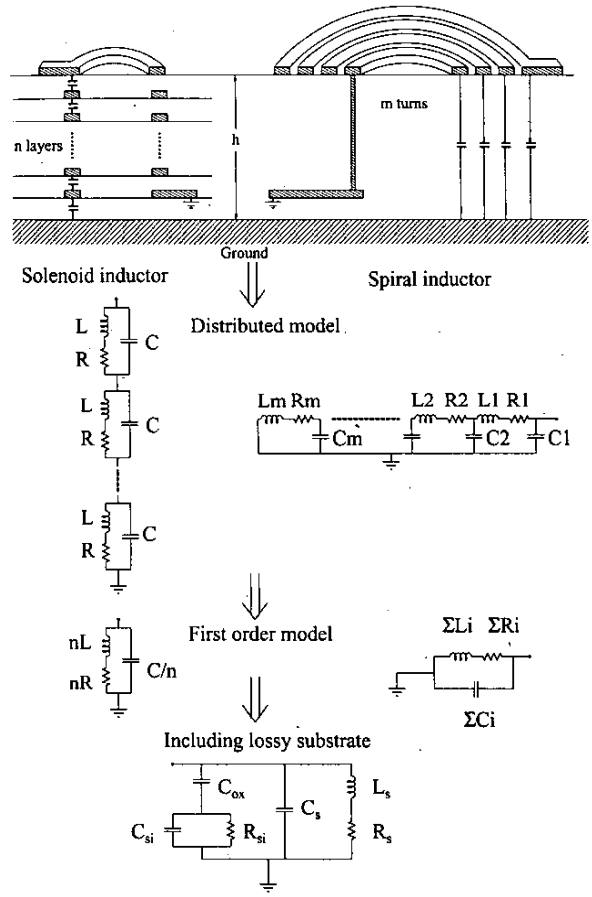

Fig. 4 Simple lump model for solenoid and spiral inductors. The parasitic capacitance of the solenoid inductor is dominated by inter-metal capacitance Cs = C/n. The parasitic capacitance of the spiral inductor is dominated by metal to substrate capacitance Cox = ΣCi. For same inductance, the solenoid inductor has smaller total parasitic capacitance than spiral inductor and hence higher self-resonant frequency.

III. Measurement Results

The die micrograph of the LNA is shown in Fig. 5. The LNA core consumes 0.6mA current while the Q-enhancement stage only consumes 0.3mA current from the 1.5V power supply. The power gain of the LNA including the input impedance matching network is shown in Fig. 6. The output buffer has a 24dB voltage loss when differential output pins are connected to 50Ω transmission lines. The input and output baluns contribute an additional 0.8dB loss. The effective voltage gain before the output buffer is 56.3dB. The LNA input is matched to 50Ω by a pair of transmission lines and a capacitor before being converted to a single-ended signal by the balun. The input matching

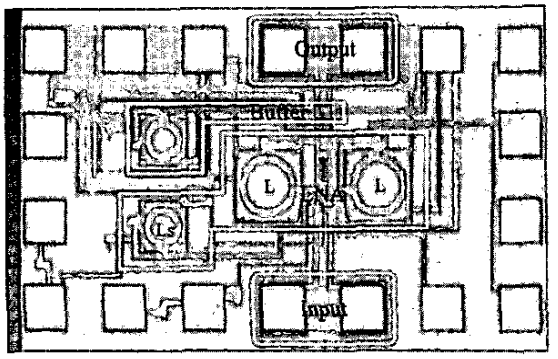

Fig. 5 Die micrograph of the LNA.

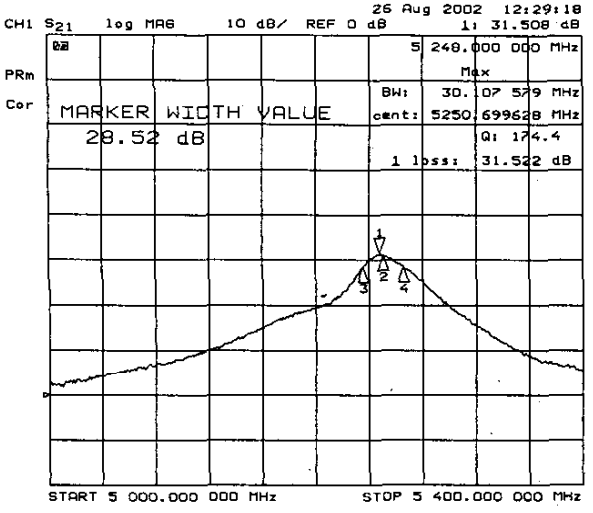

Fig. 6 The power gain of the LNA including input impedance matching network. The center frequency of the channel filter is tuned at 5.25GHz.

network provides around 15dB voltage gain. The measured S11 and S12 after impedance matching is shown in Fig. 7. The input matching network has a -3dB bandwidth of 222MHz which covers the two lower frequency bands of the 802.11a wireless LAN system. At 5.15GHz (Fig. 8) and 5.35GHz (Fig. 9), the LNA gain is reduced by about 3dB due to the LNA input bandwidth.

The filter center frequency is controlled by a 3-bit binary-weighted MOS varactor array for discrete frequency tuning. An additional LSB varactor was used for continuous fine frequency tuning which has an about 70MHz tuning range to cover three channels. Using the VCO with an identical inductor as the LNA, a master-slave control technique can be used to lock the filter center frequency as shown in Fig. 10. The frequency offset between the VCO and LNA can be cancelled by adjusting the control bits of the varactor array.

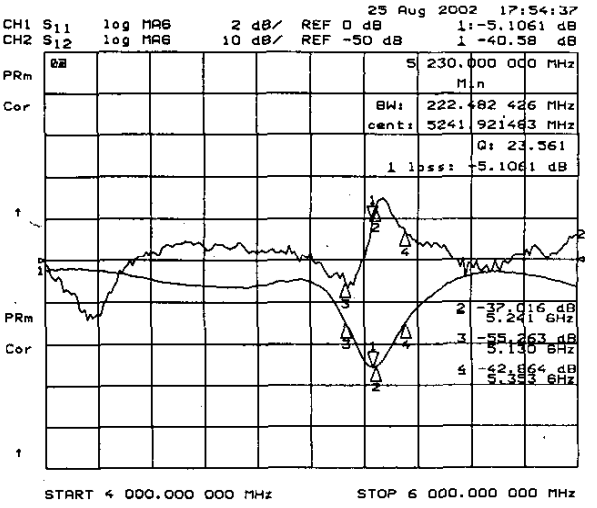

Fig. 7 Input match S11 and reverse isolation S12 of the LNA.

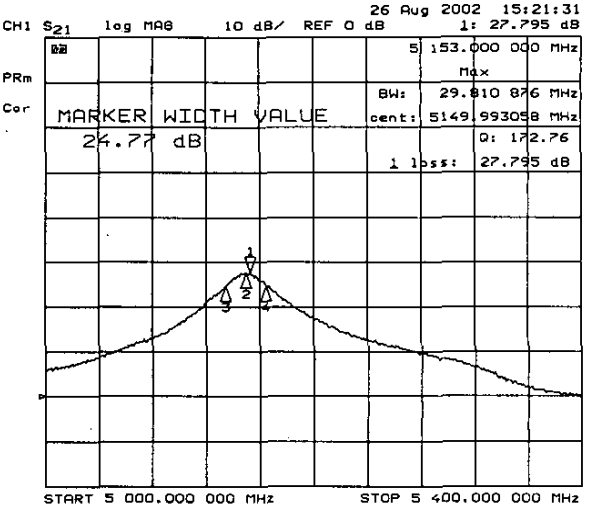

Fig. 8 The center frequency of the channel filter is tuned at 5.15GHz.

A 2-tone signal of 5.25GHz with 20kHz difference was applied to the LNA input. The output power against the input power for both fundamental signals and third order products are shown in Fig. 11. The 1dB compression point and IP3 at the buffer output are -37.7dBm and -14.7dBm respectively. Assume the output buffer does not degrade the linearity of the circuit, the effective 1dB compression point and IP3 before the buffer are 65mVpp and 900mVpp respectively. The noise figure of the LNA is 6.5dB. If the bias current of the LNA core is increased from 0.6mA to 1mA, the noise figure can be reduced by 0.5dB. The performance of the LNA is summarized in Table 1.

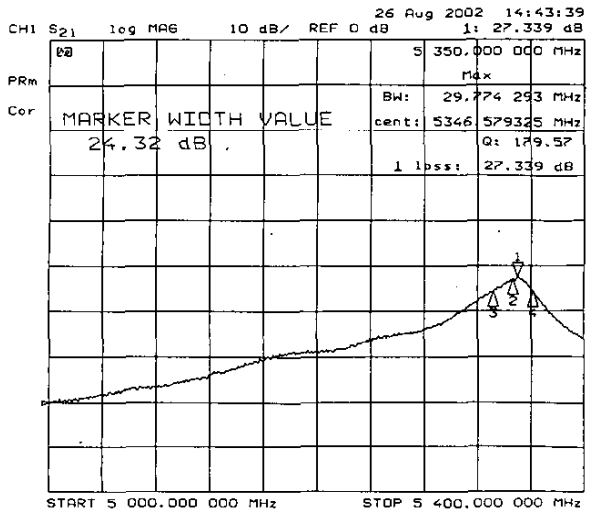

Fig. 9 The center frequency of the channel filter is tuned at 5.35GHz.

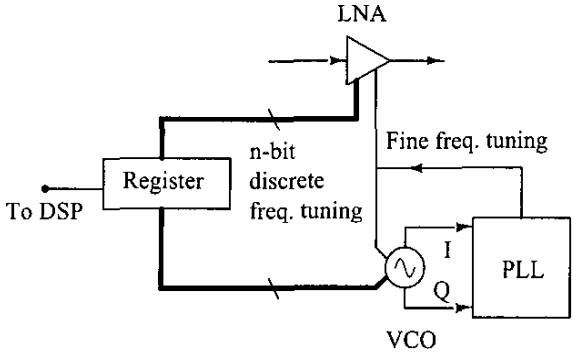

Fig. 10 Master-slave tuning scheme for LNA channel filter.

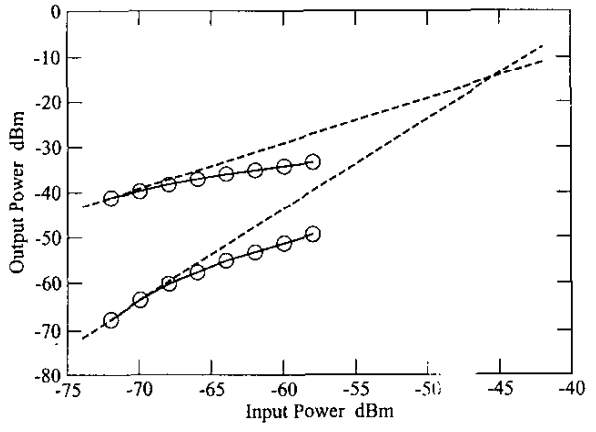

Fig. 11 The result of 2-tone test. The intersecting point gives the IP3 to be -14.7dBm at the buffer output.

Table 1: Summary of LNA performance

Process	0.18μm CMOS
Power supply	1.5V
Power dissipation	1.35mW
Voltage gain	56.3 dB before output buffer
Filter bandwidth	30MHz tunable center frequency
Input impedance match, S11	-5.1dB at 5.23GHz
Input -3dB bandwidth	222MHz
Minimum reverse isolation include buffer	35dB
1dB compression point	-37.7dBm at buffer output
IP3	-14.7dBm at buffer output
Noise figure	6.5dB

IV. Conclusion

A 5GHz 56dB voltage gain LNA with built-in tunable channel filter was designed for wireless LAN direct conversion receiver. Using compact, high quality-factor on-chip inductor, the LNA drains sub-mA current from the 1.5V power supply.

Acknowledgement

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[2] W. B. Kuhn et al, "A 200 MHz CMOS Q-Enhanced LC Bandpass Filter," IEEE J. Solid-State Circuits, vol. 31, pp. 1112-1122, August 1996.